What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate;

a gate electrode formed on the semiconductor substrate;

a low concentration impurity layer formed by introducing impurities at a low concentration into the semiconductor substrate on each side of the gate electrode;

a first insulation film formed at least on the low concentration impurity layer;

an opening provided in the first insulation film to expose part of the low concentration impurity layer;

a source/drain layer formed by introducing impurities into the low concentration impurity layer at a position aligned with the opening at a concentration higher than that of the low concentration impurity layer;

a silicide film formed by siliciding a surface of the source/drain layer;

a second insulation film formed on the semiconductor substrate to cover the gate electrode and the first insulation film;

a contact hole formed in a width larger than that of the opening at a position aligned with the opening in the second insulation film, the contact hole reaching the source/drain layer from a upper surface of the second insulation film via the opening;

a contact plug formed by filling the contact hole with electrical conductor; and

wiring formed on the second insulation film and electrically connected to the silicide film via the contact plug.

2. The semiconductor device according to claim 1, wherein the first insulation film is composed of silicon nitride, and the second insulation film is composed of silicon oxide.

3. A manufacturing method for a semiconductor device, comprising the steps of:

forming a gate electrode on a semiconductor substrate;

forming a low concentration impurity layer by introducing impurities into the semiconductor substrate at a low concentration using the gate electrode as a mask;

forming a first insulation film on the semiconductor substrate and the gate electrode, and forming an opening exposing part of the low concentration impurity layer by patterning of the first insulation film;

forming a source/drain layer by introducing impurities into the low concentration impurity layer through the opening at a concentration higher than that of the low concentration impurity layer;

forming a silicide film by siliciding a surface of the source/drain layer inside the opening;

forming a second insulation film over an entire upper surface of the semiconductor substrate;

forming a contact hole exposing the silicide film by etching the second insulation film in a width larger than that of the opening of the first insulation film;

forming a contact plug by filling the contact hole with electrical conductor; and

forming wiring on the second insulation film, the wiring being electrically connected to the silicide film via the contact plug.

4. The manufacturing method for a semiconductor device according to claim 3, wherein the first insulation film is formed of silicon nitride, and the second insulation film is formed of silicon oxide.

5. The manufacturing method for a semiconductor device according to claim 3, wherein, in the formation of the contact hole, the second insulation film is etched under a condition of high etching selectivity of the first insulation film and the second insulation film.

6. The manufacturing method for a semiconductor device according to claim 3, wherein a distance between the opening and the gate electrode is set in accordance with a withstanding voltage required for a transistor.

7. A semiconductor device, comprising:

a semiconductor substrate;

a gate electrode formed on the semiconductor substrate;

a low concentration impurity layer formed by introducing impurities at a low concentration into the semiconductor substrate on each side of the gate electrode;

a first insulation film formed on the low concentration impurity layer and the gate electrode;

an opening provided in the first insulation film, the opening exposing part of the gate electrode;

a silicide film formed by siliciding a surface of the gate electrode inside the opening;

a second insulation film formed on the semiconductor substrate to cover the gate electrode and the first insulation film;

a contact hole reaching the low concentration impurity layer from a upper surface of the second insulation film;

a source/drain layer formed by introducing impurities into the low concentration impurity layer at a position aligned with the contact hole at a concentration higher than that of the low concentration impurity layer;

a contact plug formed by filling the contact hole with an electrical conductor; and

wiring formed on the second insulation film and electrically connected to the source/drain layer via the contact plug.

8. The semiconductor device according to claim 7, wherein the first insulation film is composed of silicon nitride, and the second insulation film is composed of silicon oxide.

9. A manufacturing method for a semiconductor device, comprising the steps of:

forming a gate electrode on a semiconductor substrate;

forming a low concentration impurity layer by introducing impurities at a low concentration into the semiconductor substrate using the gate electrode as a mask;

forming a first insulation film over an entire upper surface of the semiconductor substrate, and then forming an opening exposing part of the gate electrode by patterning the first insulation film;

forming a silicide film by siliciding a surface of the gate electrode inside the opening;

forming a second insulation film over an entire upper surface of the semiconductor substrate;

forming a contact hole reaching the low concentration impurity layer from a upper surface of the second insulation film;

forming a source/drain layer by introducing impurities into the low concentration impurity layer through the contact hole at a concentration higher than that of the low concentration impurity layer;

forming a contact plug by filling the contact hole with an electrical conductor; and

forming wiring on the second insulation film, the wiring being electrically connected to the source/drain layer via the contact plug.

10. The manufacturing method for a semiconductor device according to claim 9, wherein the first insulation film is formed of silicon nitride, and the second insulation film is formed of silicon oxide.

11. The manufacturing method for a semiconductor device according to claim 9, wherein a distance between the contact hole and the gate electrode is set in accordance with a withstanding voltage required for a transistor.

12. A manufacturing method for a semiconductor device including a high voltage transistor and a low voltage transistor, comprising the steps of:

forming a first gate electrode in a formation region of the high voltage transistor of a semiconductor substrate, and forming a second gate electrode in a formation region of the low voltage transistor thereof;

forming a first low concentration impurity layer by introducing impurities at a low concentration into the semiconductor substrate using the first gate electrode as a mask, and forming a second low concentration impurity layer by introducing impurities at a low concentration into the semiconductor substrate using the second gate electrode as a mask;

forming a first insulation film over an entire upper surface of the semiconductor substrate;

forming a resist film on the first insulating layer, the resist film having an opening exposing a whole of the formation region of the low voltage transistor and part of the first insulation film on the first low concentration impurity layer;

forming an opening in the first insulation film and a sidewall on each side of the second gate electrode by

anisotropically etching the first insulation film, the opening communicating with the first low concentration impurity layer;

removing the resist film;

forming a first source/drain layer and a second source/drain layer in the first low concentration impurity layer and the second low concentration impurity layer, respectively, by introducing impurities into the first and second low concentration impurity layers at concentrations higher than those of the first and second low concentration impurity layers using the first insulation film and the sidewall as masks;

forming a first silicide film by siliciding a surface of the first source/drain layer, and forming a second silicide film by siliciding a surface of the second source/drain layer;

forming a second insulation film over the entire upper surface of the semiconductor substrate;

forming a first contact hole reaching the first silicide film from a upper surface of the second insulation film through the opening of the first insulation film, and forming a second contact hole reaching the second silicide film from a upper surface of the second insulation film;

forming contact plugs by filling the first and second contact holes with electrical conductors; and

forming wiring on the second insulation film, the wiring being connected to the contact plugs.

13. A manufacturing method for a semiconductor device including a high voltage transistor and a low voltage transistor, comprising the steps of:

forming a first gate electrode in a formation region of the high voltage transistor of a semiconductor substrate, and forming a second gate electrode in a formation region of the low voltage transistor thereof;

forming a first low concentration impurity layer by introducing impurities at a low concentration into the semiconductor substrate using the first gate electrode as a mask, and forming a second low concentration impurity layer by introducing impurities at a low concentration into the semiconductor substrate using the second gate electrode as a mask;

forming a first insulation film over an entire upper surface of the semiconductor substrate;

forming a resist film on the semiconductor substrate, the resist film having openings exposing a whole of the formation region of the low voltage transistor and part of the first insulation film on the first gate electrode;

forming an opening on the first insulation film and a sidewall on each side of the second gate electrode by anisotropically etching the first insulation film, the opening reaching the first gate electrode;

removing the resist film;

forming a first source/drain layer by introducing impurities into the second low concentration impurity layer at

a concentration higher than that of the second low concentration impurity layer using the sidewall as a mask;

forming a first silicide film by siliciding a surface of the first source/drain layer, and forming a second silicide film by siliciding a surface of the first gate electrode;

forming a second insulation film over the entire upper surface of the semiconductor substrate;

forming a first contact hole reaching the first silicide film from a upper surface of the second insulation film;

forming a second contact hole reaching the first low concentration impurity layer from the upper surface of the second insulation film;

forming a second source/drain layer by introducing impurities into the first low concentration impurity layer through the second contact hole at a concentration higher than that of the first low concentration impurity layer;

forming contact plugs by filling the first and second contact holes with electrical conductors; and

forming wiring on the second insulation film, the wiring being connected to the contact plugs.